L Number	Hits	Search Text	DB	Time stamp
-	66	Cadence and VCC and @ad < "20001017"	USPAT;	2004/03/29 14:26
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	66	Cadence and (VCC "Virtual Component Codesign") and @ad <	USPAT;	2004/03/29 14:25
		"20001017"	US-PGPUB;	
		·	EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	0	Cadence and "Virtual Component Codesign" and @ad <	USPAT;	2004/03/29 14:26
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			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	0	Cadence and "Virtual Component Codesign"	USPAT;	2004/03/29 14:26
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	0	"Virtual Component Codesign"	USPAT;	2004/03/29 14:26
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	•
-	3151	Cadence and @ad < "20001017"	USPAT;	2004/03/29 14:26
			US-PGPUB;	•
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		·	DERWENT;	
			IBM_TDB	
- ,	91	Cadence and @ad < "20001017" and "system level"	USPAT;	2004/03/29 14:27
			US-PGPUB;	
	•		EPO; JPO;	
			DERWENT;	
	_	Codeman and Sad a 112000101711 and the others levell and	IBM_TDB	2004/02/20 14:27
-	3	Cadence and @ad < "20001017" and "system level" and	USPAT; US-PGPUB;	2004/03/29 14:27
		"integration system"	EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	3	Cadence and @ad < "20001017" and "system level simulation"	USPAT;	2004/03/29 14:28
	. .	Cauchee and wad < 20001017 and System level simulation	US-PGPUB;	2001/03/23 17.20
		, '	EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	3	Cadence and @ad < "20001017" and ("system level simulation"	USPAT;	2004/03/29 14:29
		"system level simulating")	US-PGPUB;	
!		,,	EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	3	"Cadence Design Systems" and @ad < "20001017" and ("system	USPAT;	2004/03/29 14:31
		level simulation" "system level simulating")	US-PGPUB;	' '
			EPO; JPO;	
			DERWENT;	
-			IBM_TDB	
	3	"Cadence Design Systems" and @ad < "20001017" and ("system	USPAT;	2004/03/29 14:33
		level" "system-level") adj (simulation simulating simulator)	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	

•	3	"Cadence Design Systems" and @ad < "20001017" and ("system level" "system-level") adj (simulation simulating simulator) and (system cadence level simulation simulating simulator simulate model behavior capturing capture captured simulated mapping architecture wire connection component element schedule schedulable schedulator scheduling identifying identification identified message messaging messages reaction step hierarchical embedded embed consumer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/03/29 14:40
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